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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,601	07/07/2003	Abhishek Lal	852463.402	8291

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EXAMINER	
JEANGLAUDE, JEAN BRUNER	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 02/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,601	LAL, ABHISHEK	
	Examiner	Art Unit	
	Jean B. Jeanglaude	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *RCE filed on 1- 26-06*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5-14* is/are allowed.

6)☒ Claim(s) *1-4 and 15-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response To Amendments/Arguments

1. Applicant's arguments with respect to claims 1 – 24 have been considered but are moot in view of the new ground(s) of rejection.

2. Regarding the applicant's argument on page 9, first paragraph that "the control signals from the decoder 120 in Ginetti have been identified as outputs", the Examiner agrees with the applicant's argument and the examiner provides more clarification on the subject matter.

3. Regarding the applicant's argument on page 9, fourth paragraph that Ginetti does not teach or suggest "that the selected output is used to deactivate the plurality of outputs that are not selected, the Examiner maintains that Ginetti discloses such a limitation since Ginetti discloses in fig. 2 a system that receives a digital signal that is fed to a decoder, a selection circuit (130) structured to activate from a plurality of outputs (N0,..., N5) a selected output corresponding to an input binary value (fig. 2) and a deselecting circuit (130) coupled to the plurality of outputs (N0,..., N5) that deactivates the plurality of outputs except the selected output when the selected output is activated (fig. 2)[col. 4, lines 33 – 41] [as seen in fig. 2, the transistors, MN0, MN1, MN2, MN3, MP0, MP1, MP2, MP3 are used to select the output of each nodes that is reproduced as Voltage output at Vout. This output corresponds to the digital input of the circuitry. These transistors are also used to select and deselect a specific node].

DETAILED ACTION

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United State

5. Claims 1 – 4, 15 - 17, 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Ginetti (US Patent Number 5,831,566).

6. Regarding claims 1, 4, 15, Ginetti discloses an improved binary decoder (a binary decoder) and method (fig. 2) that comprises a selection circuit (130) structured to activate from a plurality of outputs (N0,..., N5) a selected output corresponding to an input binary value (fig. 2) and a deselecting circuit (130) coupled to the plurality of outputs (N0,..., N5) that deactivates the plurality of outputs except the selected output when the selected output is activated (fig. 2)[col. 4, lines 33 – 49] [as seen in fig. 2, the transistors, MN0, MN1, MN2, MN3, MP0, MP1, MP2, MP3 are used to select the output of each nodes that is reproduced as Voltage output at Vout. This output correspond to the digital input of the circuitry. These transistors are also used to select and deselect a specific node].

7. Regarding claims 2, 16, Ginetti discloses an improved binary decoder [decoder] (fig. 2) wherein the selection means (130) comprises a circuit arrangement of gates (the transistor have gates) for selecting a desired output (fig. 2).

8. Regarding claims 3, 17, Ginetti discloses an improved binary decoder [decoder] (fig. 2) wherein the deselecting means (130) comprises a circuit arrangement (the transistors) having a single input (Vss) connected to the selected output of the selection

means (fig. 2) and a plurality of outputs (N0,..., N5) of which is connected to one of the remaining outputs of the selection means, such that when the input of the circuit arrangement is activate all the other outputs of the decoder are forced to the inactive state (fig. 2)[col. 4, lines 33 – 49] [as seen in fig. 2, the transistors, MN0, MN1, MN2, MN3, MP0, MP1, MP2, MP3 are used to select the output of each nodes that is reproduced as Voltage output at Vout. This output correspond to the digital input of the circuitry. These transistors are also used to select and deselect a specific node]..

9. Regarding claim 24, Ginetti discloses a decoder (fig. 2) wherein the selection circuit (130) includes a first transistor (MN3) coupled between a reference voltage (Vss) and a first one of the outputs (the node by Ro leading to MN3); and a second transistor (MN2) coupled between the reference voltage and a second one (N3) of the outputs wherein the deselection circuit (130) includes a third transistor (MP3) connected between the reference voltage (VDD) and the first output and having an input connected to the second output and a fourth transistor connected between the reference voltage and the second output having an input connected to the first output (fig. 2)[as noted in fig. 2, the transistors are used to select and deselect the outputs of the decoder 120] (see col. 4, lines 33 – 49] [as seen in fig. 2, the transistors, MN0, MN1, MN2, MN3, MP0, MP1, MP2, MP3 are used to select the output of each nodes that is reproduced as Voltage output at Vout. This output correspond to the digital input of the circuitry. These transistors are also used to select and deselect a specific node].

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 18, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ginetti (US Patent Number 5,831,566) in view of the Applicant's admitted prior art (APA).

12. Regarding claims 18, 19, Ginetti discloses all the limitations as discussed above except the decoder wherein the selection and deselection circuits are connected to provide a 2-to 4 decoder that provides an active low output for an input of A'.B' and for an input A.B' (claim 18) and a decoder wherein the selection and deselection circuits are connected to provide a 2-to-4 decoder that provides an active low output for an input of A'.B and for an input A.B. (claim 19). However, the APA discloses a binary decoder (decoder) wherein the selection and deselection circuits are connected to provide a 2-to 4 decoder that provides an active low output for an input of A'.B' and for an input A.B' (figs. 1 - 4) and a decoder wherein the selection and deselection circuits are connected to provide a 2-to-4 decoder that provides an active low output for an input of A'.B and for an input A.B. (figs. 1 – 4). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ginetti's system with that of the APA in order to improve the performance of the system.

13. Claims 20 - 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ginetti (US Patent Number 5,831,566) in view of Park (US Patent Number 5,844,515).

14. Regarding claims 20 – 23, Ginetti discloses all the limitations discussed above except the decoder wherein the selection and deselection circuits are connected to provide a 3-to-8 decoder that provides an active low output for an input of A'.B.C' and for an input A.B.C' (claim 20); the decoder wherein the selection and deselection circuits are connected to provide a 3-to-8 decoder that provides an active low output for an input of A'.B'.C and for an input A.B'.C (claim 21) and the decoder wherein the selection and deselection circuits are connected a 3-to-8 decoder that provides an active low output for an input of A'.B.C' and for an input A.B.C' (claim 22). However, 3-to-8 decoder is known in the art. One particular example of a known 3-to-8 decoder is the one described in Park which has three inputs and 8 outputs (decoders 30, 50 are 3-to-decoder; the logical inputs of the decoders 30, 50 are combined to produce the outputs). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to couple the decoder described in Park's system to Ginetti's system in order to provide an accurate DAC.

Allowable Subject Matter

15. Claims 5 – 14 are allowable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B. Jeanglaude whose telephone number is 571-272-1804. The examiner can normally be reached on Monday - Friday 7:30 A. M. - 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jean Bruner Jeanglaude
Primary Examiner
February 6, 2006